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Hardware Implementation and Analysis of Sinusoidal PWM-Based Three-Level Cascaded H-Bridge Inverter

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***Abstract*—Multilevel Inverter (MLI) technology is essential in medium-voltage and high-power applications as it is capable of generating high-quality AC output from multiple DC voltage sources. Among the various topologies, the Cascaded H-Bridge (CHB) MLI is preferred owing to its modularity. The conventional Neutral Point Clamped (NPC) and Flying Capacitor (FC) MLIs suffer from uneven voltage distribution, requirement of clamping diodes, and complex circuitry. To address these drawbacks, a Three-Level Sinusoidal Pulse Width Modulation (TL-SPWM)-based CHB-MLI is proposed with an inexpensive Insulated Gate Bipolar Transistor (IGBT) driver circuit and a Schmitt trigger-based dead-time circuit that introduces a one-microsecond delay at a 2 kHz switching frequency. Simulation and hardware verification confirm that the proposed system achieves significant performance improvement, reducing Total Harmonic Distortion (THD) from 48% to 31% as the modulation index is increased from 0.6 to 0.9. Experimental results show a similar reduction from 53% to 35%, with weighted THD reduced to 1.3%. These improvements confirm the effectiveness of the TL-SPWM technique in producing improved output waveform quality. The proposed inverter is well suited for renewable energy system applications, electric vehicle drives, and industrial motor drives. In addition to overcoming limitations of conventional MLI designs, this work also contributes to the further evolution of efficient and cost-effective MLI technology for real-world power electronics applications.**

Keywords—Multilevel Inverter; Cascaded H-Bridge; Sinusoidal PWM; Total Harmonic Distortion; IGBT Driver Circuit.

I. INTRODUCTION

Multilevel Inverter (MLI) technology has gained prominence in recent power electronics due to its capability to produce high-quality AC output for medium-voltage and high-power applications. By synthesizing stepped waveforms through multiple DC sources, MLIs offer advantages such as reduced Total Harmonic Distortion (THD), improved efficiency, and reduced electromagnetic interference. Among the various MLI topologies, the Cascaded H-Bridge (CHB) inverter stands out due to its modularity, ease to scale, and low component count [1]. However, conventional topologies like Neutral Point Clamped (NPC) and Flying Capacitor (FC) inverters are faced with great challenges. NPC inverters suffer from uneven voltage sharing and require a high number of clamping diodes, complicating the design and making it costly. FC inverters are faced with capacitor imbalance and bulky configurations, affecting reliability and scalability. Conventional modulation techniques are also faced with effectively controlling dead-time, leading to shoot-through faults and compromised system performance [2]. To eliminate these drawbacks, this study proposes an SPWM-based CHB MLI with a novel low-cost IGBT driver circuit and an external Schmitt trigger-based dead-time control circuit. The proposed system achieves precise pulse control, introduces a dead-time of one microsecond at 2 kHz switching frequency, and reduces the likelihood of short-circuit faults [3], [4].

A. Research Gaps

Conventional Multilevel Inverter (MLI) topologies, such as Neutral Point Clamped (NPC) and Flying Capacitor (FC) inverters, face significant limitations that hinder performance in advanced power electronics applications. High Total Harmonic Distortion (THD) arises from uneven voltage distribution and capacitor imbalance. Their designs are complex, involving numerous components like clamping diodes and capacitors, increasing size, cost, and reducing scalability [5]. Traditional modulation techniques, including basic SPWM, fail to optimize switching losses effectively, lowering efficiency. Moreover, inadequate dead time control increases the risk of shoot-through faults, compromising reliability. Many medium-voltage MLI applications suffer from voluminous configurations and poor modularity, making them challenging to implement [6]. While simulation studies advance MLI research, experimental validation of improved topologies remains limited, leaving practical capabilities underexplored. This research bridges these gaps by proposing a CHB-MLI with a new SPWM technique and IGBT driver circuit, achieving lower THD, higher efficiency, and reliable dead time control through simulation and experimental analysis [7].

II. RELATED WORK

R. Wang, L. Ai, and C. Liu [8] present a DO-NPC-TLI with two independent AC voltage outputs of variable frequency and amplitude. Added novelty consists of eight additional switches and six clamping diodes in the conventional Neutral-Point-Clamped topology, in addition to a modulation strategy that combines time-sharing modulation

with Virtual Space Vector PWM. Experimental results prove the feasibility, but an increased component count introduces complexity, while VSVPWM remains computationally intensive. B. S. Gehrke et al. [9] propose single-phase three-wire systems with Two-Level and Three-Level NPC legs for the implementation of four different converters. For such converters, a novel DC-link voltage balancing approach based on Space Vector PWM has been presented which could be extended for operation within microgrids characterized by low harmonic distortion and semiconductor losses. Efficiency during unbalanced loads is an area for further study. It has to be discussed how to develop such solutions into more powerful units.

S. R. P et al. [10] present Phase Disposition (PD), Phase Opposite Disposition (POD), and Alternate Phase Opposite Disposition (APOD) PWM techniques in order to reduce THD for multilevel inverters. Simulations and hardware prototypes can identify the optimal method, but relying on software-generated code has made implementing complex PWM techniques cumbersome in hardware. P. Kalkal and A. V. R. [11] Teja proposed the Second-order Sliding Mode Controller for the solution of SHE PWM, providing chattering-free and robust convergence. Higher-order sliding mode control, despite being computationally efficient, still remains resource-intensive for high-frequency switching. L. D. Benedetto et al. [12] proposed a digital controller for SVPWM modulation. This paper is about the development of a digital controller that will implement SVPWM modulation and allow an optimal evaluation of dwell-time with reduced hardware requirements. However, scalability for advanced applications is still limited. Minimum stator current asynchronous PWM was proposed by L. Wang et al. [13] for high-speed brushless DC drives based on the gradient descent method. While efficient, it suffers from a large computational burden and limitations of commutation angle, hence limiting applications.

A. *Efficient Three-Level H-Bridge Inverter for AC Voltage Generation*

Fig. 1 topology of three-phase three-level H-bridge inverter: Each phase contains an H-bridge with four switches, such as (e.g., $S_{1a}, S_{2a}, S_{3a}, S_{4a}$ for Phase R) and correspondingly pre-assigned diodes. the DC voltage (V_{dc}) is converted into the three-phase AC output voltages for the R, Y, and B phases [14]. The following configuration allows the positive, negative, and zero voltage levels to be produced through proper control of the ON/OFF states of the switches. In the R-phase, for example, switches S_{1a} and S_{3a} conduct to produce a positive voltage, while switches S_{2a} and S_{4a} conduct to produce a negative voltage. When a zero-voltage output is required, either switches S_{1a} and S_{2a} or switches S_{3a} and S_{4a} are turned on together [15].

The inverter topology discussed here provides complete isolation of modularity of the DC sources in every phase [16]. Therefore, any unit of H-bridge units can be serviced without interference to other phases, thus enhancing the overall reliability. Further, the three-level structure ensures that the THD of the output waveform is very low, ensuring good quality AC power suitable for medium-voltage applications. The above topologies find broad applications in renewable energy systems such as solar and wind power and in industrial motor drives. The motive for the use of such topologies is the improvement in efficiency, reduction of switching losses, and improved waveform quality compared to conventional inverter counterparts [17].

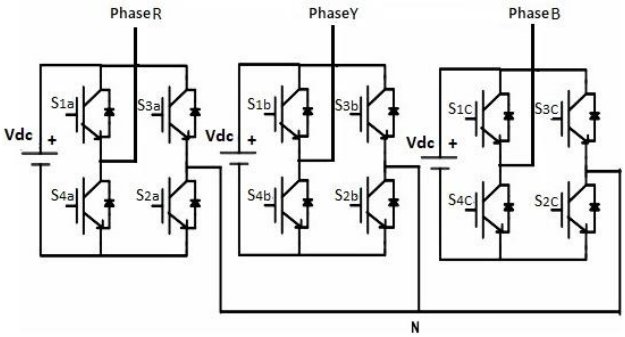


Fig. 1. Three-phase three-level H-Bridge inverter topology

B. *Reference and Carrier Wave Comparison for Switching States*

The switching states of a three-level H-Bridge inverter, compared to two triangular carrier waveforms, $V_{\text{ref}}(t)$ generate a sinusoidal reference voltage $V_{\text{carrier1}}(t)$ given by Equation (1).

$$S_i(t) = \begin{cases} +1 & \text{if } V_{\text{ref}}(t) > V_{\text{carrier1}}(t) \\ 0 & \text{if } V_{\text{carrier2}}(t) < V_{\text{ref}}(t) \le V_{\text{carrier1}}(t) \\ -1 & \text{if } V_{\text{ref}}(t) \le V_{\text{carrier2}}(t) \end{cases} \quad (1)$$

where $S_i(t)$ determines the switching state for each phase [18].

C. *Output Voltage for Each H-Bridge Phase*

The output voltage at the load terminals due to switching states in a single phase of H-Bridge is given in Equation (2).

$$V_{\text{phase}} = \begin{cases} +\frac{V_{\text{dc}}}{2} & \text{if switches } S_1 \text{ and } S_4 \text{ are ON} \\ -\frac{V_{\text{dc}}}{2} & \text{if switches } S_2 \text{ and } S_3 \text{ are ON} \\ 0 & \text{if complementary states or inactive condition} \end{cases} \quad (2)$$

where V_{dc} is the DC input voltage [19].

D. *Three-Phase AC Output Voltage*

The inverter produces a three-phase AC output $V_{\text{out, AC}}(t)$ due to such combinations of the phase voltages to determine Equation (3).

$$V_{\text{out, AC}}(t) = V_{\text{R}}(t) + V_{\text{Y}}(t) + V_{\text{B}}(t) \quad (3)$$

where $V_{\text{R}}, V_{\text{Y}}$, and V_{B} represent the respective phase voltages for R, Y, and B phases, calculated based on their individual switching states [20]-[25].

E. *Block Diagram for Reference and Carrier Signal Generation in Three-Level Inverter*

Fig. 2 sinusoidal PWM three-phase, three-level inverter signal generator circuit; there are three sine reference signals for R-phase, Y-phase, and B-phase of a three-phase system. A modulation block adjusts the modulation index to control amplitude and harmonic content [26]. Reference signals are compared with two triangular carriers "Upper Triangle" and "Lower Triangle" split symmetrically, so as to ensure that

accuracy in the generation of switching pulses will be availed. This will ensure that the accurate PWM signals are generated to the inverter output [27].

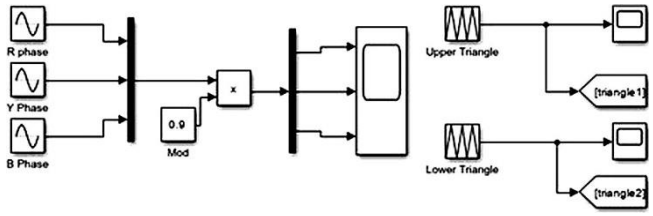


Fig. 2. Signal generation circuit for sinusoidal PWM in three-phase inverter

The comparator outputs such signals that provide the gate control signals the switches in the inverter circuit require [28]. With sufficient modulation and synchronization of reference signals with respect to carrier signals, minimum THD is guaranteed while a high-quality AC waveform output is obtained from the proposed scheme. This is the methodology that finds its centrality in applications that require effectiveness and accuracy in power conversions, such as renewable power conversion systems and motor drives [29].

F. Switching Pulse Generation Circuit for Three-Level Inverter

Fig. 3 illustrates the switching pulse generation circuit for the three-level inverter supplying the PWM signals $S_{r1}, S_{r2}, S_{r3}, S_{r4}$ to drive the switches [30]. A reference signal (mr1) is compared with two symmetric, level-shifted triangular carriers [triangle1 and triangle2].

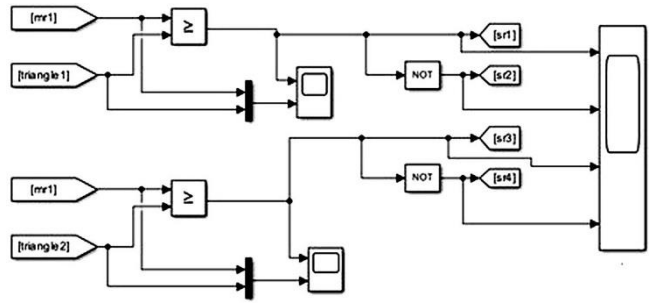


Fig. 3. Block diagram for generating complementary PWM signals in three-level inverter

Comparators perform the comparison of reference and carrier signals to develop the switching transitions. Outputs are fed through the NOT gates to develop the complementing signals at each switch pair. As an example, S_{r1} and S_{r2} and so on for S_{r3} and S_{r4} are always making sure that one turns off while the other is turning on in order to avoid short circuiting [31]-[35].

G. Synchronization of Reference and Carrier Waves in PWM Modulation

Fig. 4 shows the reference and carrier waveforms for PWM in a three-level inverter: a sinusoidal reference wave (black) and symmetric, level-shifted triangular carriers (blue and red). By comparing the reference wave with the carriers, switching pulses are obtained that generate a stepped AC output approximating the sinusoidal waveform. Because of this process, harmonic distortion is very small. Synchronism between reference and carriers ensures high-quality output voltage with low THD-a factor applied in wide applications in renewable energy and motor drives for efficient power conversion [36]-[46].

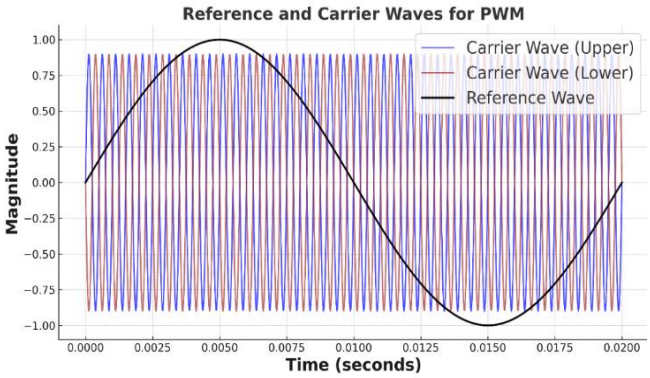


Fig. 4. Reference and carrier waveforms for PWM signal generation

H. Reference, Carrier, and Switching Pulse Waveforms for Three-Phase Three-Level Inverter

Fig. 5 shows the generation of a waveform in three-level inverter with sinusoidal Pulse Width Modulation: the top sub window has the triangular carrier waveforms of upper and lower symmetric used for PWM modulation [47]-[62].

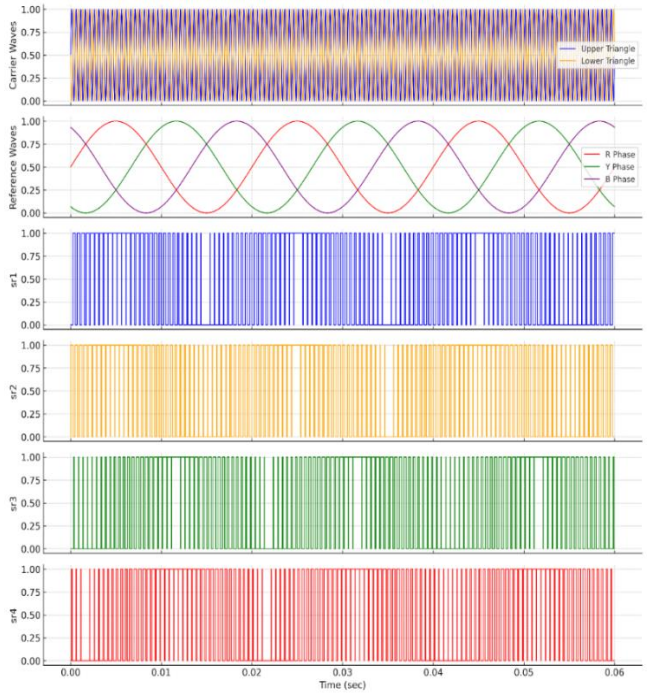


Fig. 5. Waveform analysis for PWM signal generation in three-level inverter

In reality, such carrier signals are required in establishing switching points through a comparison with sinusoidal reference signals [63]-[70].

The second panel shows the waveforms of three phases (R, Y, B) sinusoidal references [71]-[75]. These signals are the reference or desired AC output voltage for each phase and are in-phase with each other to provide balanced three-phase output. the switching signals $S_{r1}, S_{r2}, S_{r3}, S_{r4}$ for the inverter switches. The signals will be obtained by comparing the reference waves with the carrier waves [76]-[81].

I. Methodology of TL-SPWM-Based CHB Inverter

Fig. 6 depicts the sequential methodology for the implementation of the presented TL-SPWM-based Cascaded H-Bridge (CHB) inverter. It starts with generation of reference sine signals for individual phases, followed by comparison of these with level-shifted carrier signals for generation of TL-SPWM pulses. It incorporates a Schmitt trigger-based circuit for adding controlled dead-time for shoot-through protection. TL-SPWM pulses are utilized for driving IGBT switches, leading to controlled three-level inverter operation and generation of output waveform. The performance of the system is tested through Total Harmonic Distortion (THD) analysis.

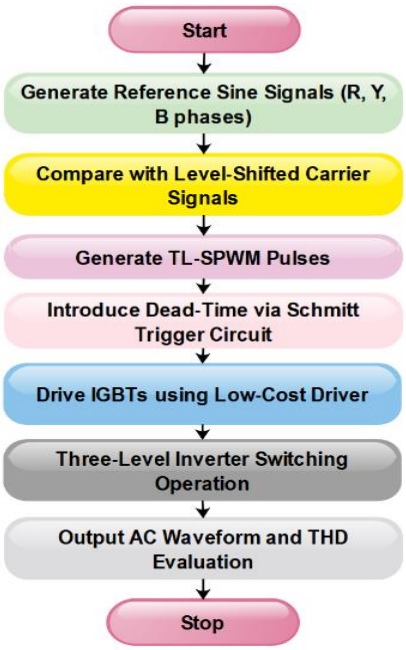


Fig. 6. Methodology flowchart for TL-SPWM-based CHB inverter

III. HARDWARE SETUP FOR THE PROPOSED TL-SPWM-BASED THREE-LEVEL H-BRIDGE INVERTER

Fig. 7 depicts the experimental validation of the proposed methodology in hardware setup for the Three-Level Sinusoidal Pulse Width Modulation (TL-SPWM) -based H-Bridge Inverter. The H-bridge inverter is powered from an isolated supply as a DC voltage source input to generate multi-level output from the inverter. Also, DC power is feeding to the inverter provided by an AC-DC rectifier. The micro-controller generates the TL-SPWM signals for precise IGBT switching to generate a three-step staircase AC waveform with reduced total harmonic distortion.

A dead-time circuit that includes the Schmitt trigger now introduces a delay of 1 microsecond at the 2 kHz switching frequency of the inverter power transistors to eliminate the shoot-through faults and allow for efficient operations. In this case, it uses a motor connected to act as the load while performing clean, stable AC output demonstration.

Therefore, such a setup confidently confirms that the TL-SPWM technique, low-cost IGBT driver, and Schmitt trigger-based dead-time circuit are effective means to achieve higher quality waveforms with extremely low THD, thus proving the reliability of the methodology.

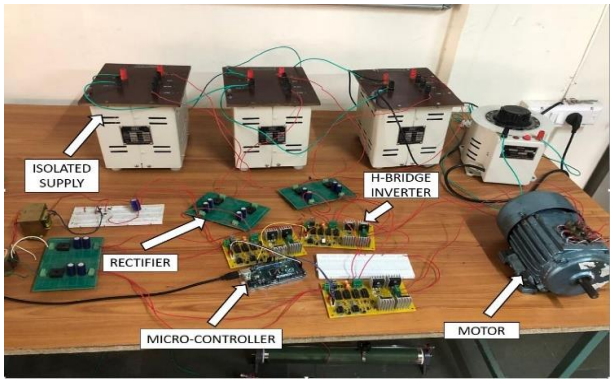


Fig. 7. Hardware setup for the proposed TL-SPWM-based three-level H-bridge inverter

A. Reference Voltage for Each Phase

The reference voltage defines the sinusoidal waveform for each phase of the inverter and it is determined by Equation (4).

$$V_{\text{ref}}(t) = V_m \sin(\omega t) \tag{4}$$

Where $V_{\text{ref}}(t)$ is the reference voltage at time t, V_m is the peak value of the reference voltage, ω is the angular frequency ($\omega = 2\pi f$) and t is the time variable.

B. Carrier and Reference Comparison for PWM

The Pulse Width Modulation (PWM) switching signals are generated by comparing the sinusoidal reference voltage with level-shifted triangular carrier waveforms and it calculated by Equation (5).

$$S_{\text{pulses}} = \begin{cases} 1 & \text{if } V_{\text{ref}} > V_{\text{carrier, upper}} \\ 0 & \text{if } V_{\text{ref}} < V_{\text{carrier, lower}} \end{cases} \tag{5}$$

Where, S_{pulses} is the switching pulse signal, V_{ref} is the reference sinusoidal voltage, $V_{\text{carrier, upper}}$ is the upper triangular carrier waveform voltage, and $V_{\text{carrier, lower}}$ is the lower triangular carrier waveform voltage.

C. Output Voltage for Each Phase

The output voltage at the load terminals of a single-phase H-Bridge inverter depends on the switch states and its calculated using Equation (6).

$$V_{\text{out}}(t) = \begin{cases} +V_{\text{dc}} & \text{if switches } S_1 \text{ and } S_4 \text{ are ON} \\ 0 & \text{if switches } S_1 \text{ and } S_3 \text{ (or } S_2 \text{ and } S_4\text{) are ON} \\ -V_{\text{dc}} & \text{if switches } S_2 \text{ and } S_3 \text{ are ON} \end{cases} \tag{6}$$

Where, $V_{\text{out}}(t)$ is the output voltage of the inverter, V_{dc} is the isolated DC voltage source, and S_1, S_2, S_3, S_4 are the switching states of the inverter switches.

D. Output Voltage for Three-Phase Inverter

The total output voltage of the three-phase inverter is the combination of voltages from all three H-Bridge phases and it calculated by Equation (7).

$$V_{\text{phase}} = V_{\text{out, R}} + V_{\text{out, Y}} + V_{\text{out, B}} \tag{7}$$

Where, V_{phase} is the total three-phase inverter output voltage, $V_{\text{out, R}}$ is the output voltage of the R-phase, $V_{\text{out, Y}}$ is the output voltage of the Y-phase, and $V_{\text{out, B}}$ is the output voltage of the B-phase.

E. Total Harmonic Distortion (THD)

The THD quantifies the harmonic distortion in the inverter output compared to the fundamental voltage component and it is calculated by Equation (8).

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100\% \quad (8)$$

Where, THD is the Total Harmonic Distortion (%), V_n is the RMS voltage of the n^{th} harmonic component, and V_1 is the RMS voltage of the fundamental component.

F. Power Delivered to the Load

The power delivered to an inductive load is calculated using the RMS voltage and load resistance and it is determined by the Equation (9).

$$P = \frac{V_{\text{rms}}^2}{R} \quad (9)$$

Where, P is the power delivered to the load (Watts), V_{rms} is the RMS value of the inverter output voltage, and R is the load resistance.

Fig. 8 shows the external dead-time circuit for the TL-SPWM-based H-Bridge Inverter, designed to prevent shoot-through faults. An optocoupler (6N137) isolates the input PWM signal, maintaining signal integrity. An RC network (1kΩ resistor and 1nF capacitor) introduces a delay based on the RC time constant, ensuring the required dead-time.

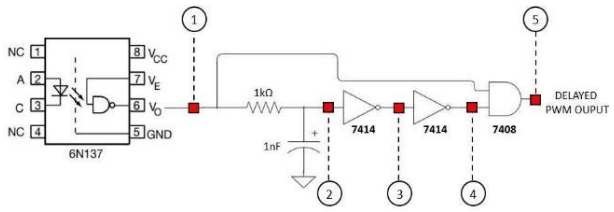


Fig. 8. External dead-time circuit for TL-SPWM-based three-level H-bridge inverter

The delayed signal passes through Schmitt triggers (IC 7414) to sharpen edges and an AND gate (IC 7408) to generate precise delayed PWM outputs. This design provides a 1-microsecond dead-time, preventing simultaneous conduction in the same leg, ensuring reliable operation at a 2kHz switching frequency.

G. Dead-Time Delay Waveform for TL-SPWM-Based Three-Level H-Bridge Inverter

The dead-time delay waveform in the TL-SPWM-based H-Bridge Inverter is shown in the Fig. 9. Channel 1 (CH1) illustrates the high-side gate pulse, while Channel 2 (CH2) is the low-side gate pulse. A dead-time delay between the rising edges of pulses ($\Delta t = 1.08\,\mu s$) was implemented to avoid simultaneous conduction in the same leg and to prevent shoot-through faults.

The Schmitt trigger-based circuit along with the RC filter allows precise timing control with a delay of 1 microsecond at a switching frequency of 2kHz. Voltage difference ΔV = 5.12V provides the proper gate pulse amplitude. Validation of the waveform shows the effectiveness of the approach for the reduction of THD and improvement in the quality of the output.

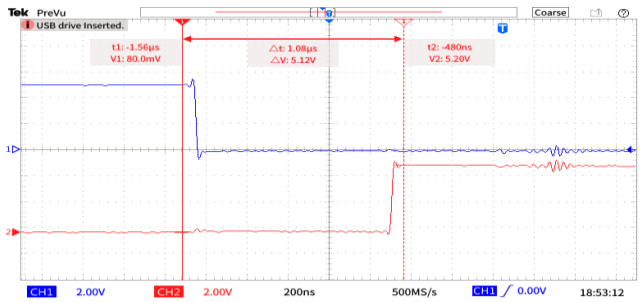


Fig. 9. Dead-time delay waveform for TL-SPWM-based three-level H-bridge inverter

IV. Simulation and Experimental Validation of the Proposed TL-SPWM-Based Three-Level H-Bridge Inverter

Table I summarizes the key hardware parameters and component specifications used in the experimental validation of the proposed inverter system, including switching frequency, dead-time delay, load characteristics, and Schmitt trigger-based delay circuit configuration.

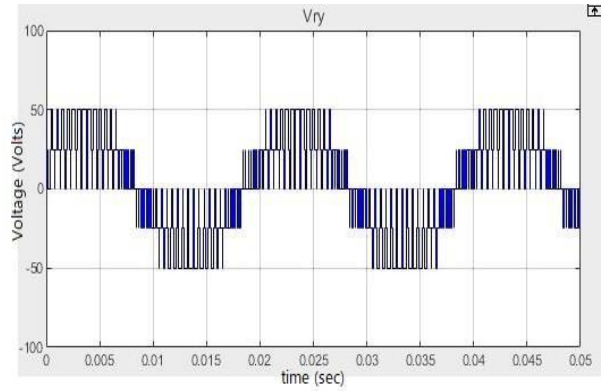
TABLE I. Experimental Setup Parameters for TL-SPWM-Based Three-Level H-Bridge Inverter

Parameter	Value
Switching Frequency	2 kHz
Dead Time Delay (Δt)	1.08 µs
Load Specifications	150 Ω, 100 mH
Schmitt Trigger RC Network	R = 1 kΩ, C = 1 µF
Dead-Time Control Technique	Schmitt trigger-based RC delay circuit
PWM Technique	Three-Level Sinusoidal PWM (TL-SPWM)

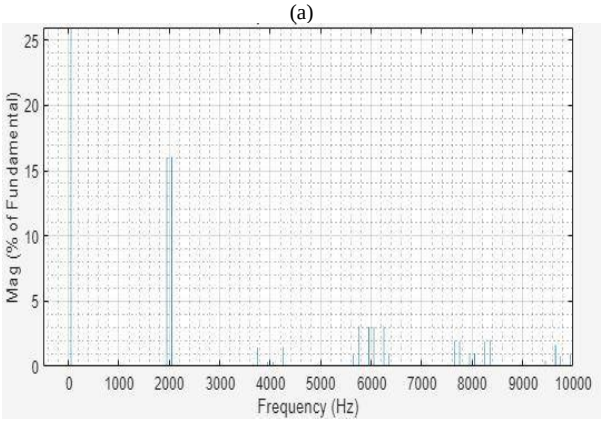
The simulation and experimental validation of the TL-SPWM-based H-Bridge Inverter. Simulated output voltage waveform and FFT analysis at M = 0.6 are presented in Fig. 10 (a) and (b) respectively. In this case the THD is 48%. Experimental validation of the results showing similar levels of THD is presented in Fig. 11 (a) and (b). For M = 0.9, Fig. 12 (a) and (b) depict a simulated THD reduction to 31%, while Fig. 13 (a) and (b) confirm this experimentally. Waveforms are now less harmonic and with better quality output voltage since the modulation index is increased. The proposed TL-SPWM method, in combination with the Schmitt trigger-based dead-time circuit, ensures reliable and precise switching of the IGBT driver circuit. Both simulation and experimental findings validate the effectiveness of the proposed method in minimizing THD and achieving a high-quality output waveform.

A. Experimental Setup – Assumptions and Limitations

It assumes ideal conditions for operation, such as correct timing of the Schmitt trigger-dead-time circuit and linear load behavior. It tests under constant laboratory conditions on a resistive-inductive load of 150 Ω, 100 mH, assuming that such a representation exists in real industry. It only tests with two modulation indices of 0.6 and 0.9, and environmental conditions such as temperature changes are not catered for. The precision of the RC loads also may fluctuate, impacting the dead time. It also does not cater for switching at higher frequencies or sophisticated digital control boards, which will be addressed in later work.

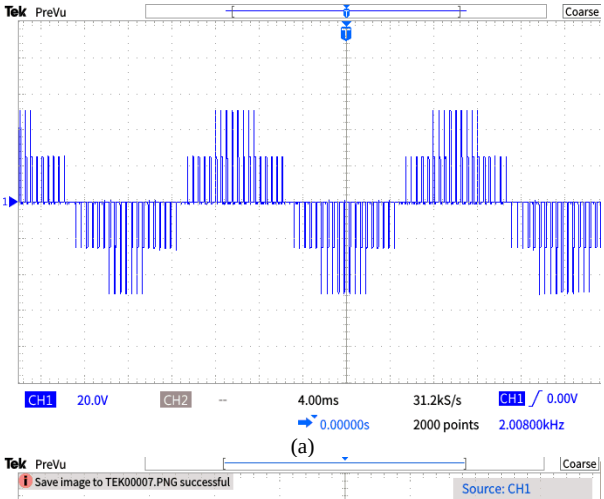


(a)



(b)

Fig. 10. Simulated result for three level MLI (a) Output Voltage Waveform (b) Harmonic Spectrum at M=0.6



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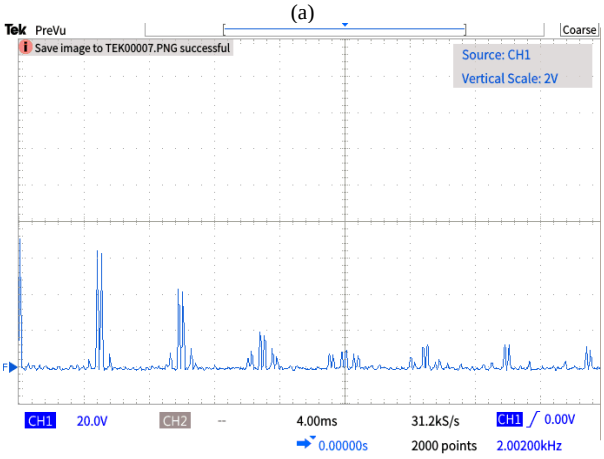
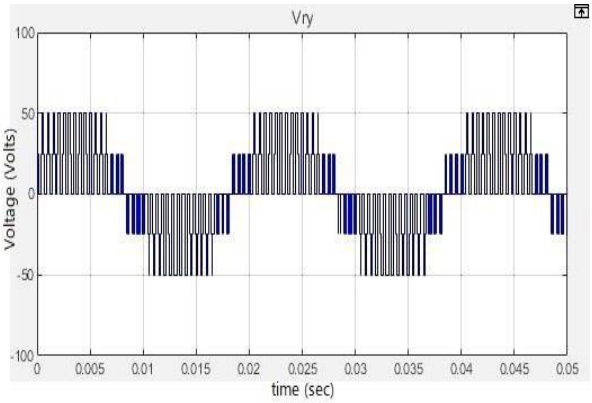


(b)

Fig. 11. Experimental result for three level MLI (a) Output Voltage Waveform (b) Harmonic Spectrum at M=0.6



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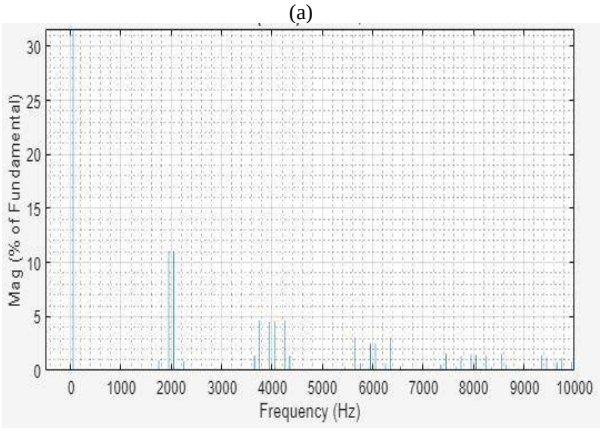
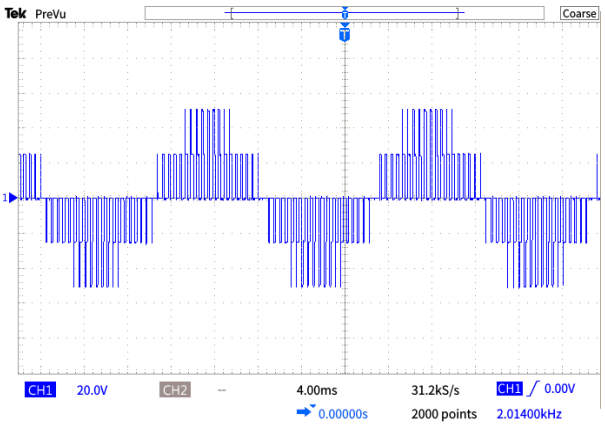


(b)

Fig. 12. Simulated result for three level MLI (a) Output Voltage Waveform (b) Harmonic Spectrum at M=0.9



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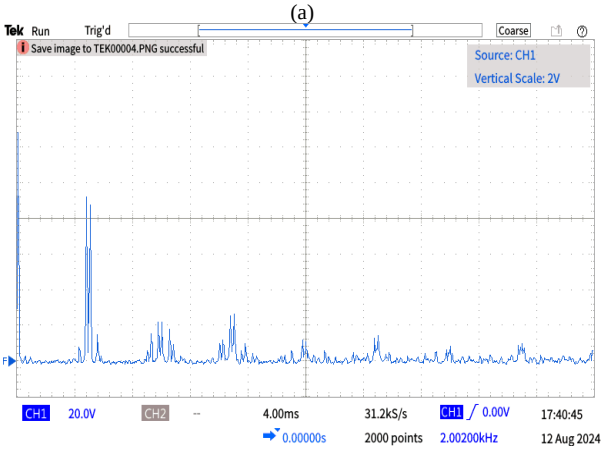

(b)

Fig. 13. Experimental result for three level MLI (a) Output Voltage Waveform (b) Harmonic Spectrum at M=0.9

B. Impact of External Factors on Circuit Performance

Performance of the intended TL-SPWM-based inverter will be affected by several external factors like temperature fluctuations, component tolerances, and electromagnetic interference (EMI). Temperature variations will influence the response of passive components like resistors and capacitors in the dead-time circuit, the intended delay time, and thus timing mismatches. Component tolerances will also produce pulse width generation and output waveform quality inconsistencies. EMI will affect the integrity of signals, particularly under high-frequency switching conditions. Even though these factors have not been thoroughly studied under the present configuration, they are critical regions for further research towards increasing real-time reliability and robustness of the system.

Table II shows a comparison of Total Harmonic Distortion (THD) and Weighted THD for Sine PWM at modulation indices $m = 0.6$ and $m = 0.9$. For $m = 0.6$, simulation and experimental THD are 48% and 53%, with a weighted THD of 2%. At $m = 0.9$, THD reduces to 31% (simulation) and 35% (experimental), with a weighted THD of 1.3%. This highlights improved performance with increased modulation index.

TABLE II. COMPARISON OF TOTAL HARMONIC DISTORTION (THD) AND WEIGHTED THD FOR SINE PWM

Sine PWM	THD (Simulation)	THD (Experimental)	Weighted THD
m = 0.6	48%	53%	2%
m = 0.9	31%	35%	1.3%

Fig. 14 shows the comparison of Total Harmonic Distortion (THD) and Weighted THD for Sine PWM at modulation indices $m = 0.6$ and $m = 0.9$. It illustrates the THD values obtained through simulation and experimental methods, along with the weighted THD percentages. For $m = 0.6$, the simulation THD is 48%, and the experimental THD is slightly higher at 53%, with a weighted THD of 2%. For $m = 0.9$, the simulation THD decreases to 31%, and the experimental THD is 35%, with a weighted THD of 1.3%. This indicates that increasing the modulation index reduces harmonic distortion, enhancing system performance.

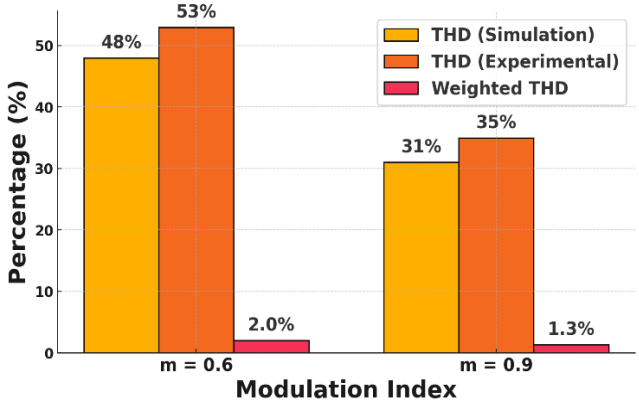

Fig. 14. Comparison of Total Harmonic Distortion (THD) and Weighted THD for Sine PWM

V. CONCLUSION

This research study successfully presents the hardware design and analysis of Three-Level Sinusoidal PWM (TL-SPWM)-driven Cascaded H-Bridge Multilevel Inverter (CHB-MLI) that resolves some of the key problems of the current inverter topologies including Neutral Point Clamped (NPC) and Flying Capacitor (FC) inverters. These current designs are beset by high Total Harmonic Distortion (THD), complex circuits, and poor dead-time control. The system here integrates an economical IGBT driver and a Schmitt trigger-based dead-time circuit that offers an accurate 1-microsecond delay at 2 kHz, successfully eradicating the occurrence of shoot-through faults and optimizing switching performance.

Experimental and simulation results verify the technique, showing appreciable reduction of THD—from 48% to 31% through simulation and from 53% to 35% through hardware. Weighted THD is also improved to 1.3%, verifying the quality of the output waveforms. The modular topology of the CHB offers greater maintainability and expandability and hence is best suited to integrate with renewable energy, electric vehicle drive, and industrial motor control. The proposed TL-SPWM-based inverter shows high-quality waveforms, high efficiency, and practical feasibility. Future research can be directed toward utilizing wide-bandgap devices like SiC or GaN to obtain better performance and applying the design to multi-phase or high-level inverter configurations using real-time digital control.

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