Journal of Robotics and Control (JRC)
Volume 2, Issue 4, July 2021
ISSN: 2715-5072 DOI: 10.18196/jrc.2487 

# Low Power NAND Gate–based Half and Full Adder / Subtractor Using CMOS Technique

Angelo A. Beltran Jr.[1], Kristina C. Nones[2], Reina Louise M. Salanguit[3],
Jay Bhie D. Santos[4], Josemaria Rei G. Santos[5], and Keith Joseph T. Dizon[6]
[1,2,3,4,5,6]Department of Electronics Engineering, Adamson University, Manila, Philippines
Email: abeltranjr@hotmail.com[1], kristinanones@gmail.com[2], reinasalanguit104@gmail.com[3], santosjay7899@gmail.com[4], jaysnts02@gmail.com[5], ktjdizon1997@gmail.com[6]

***Abstract*—In recent years, low power consumption has been an important consideration for the design of system since there is a high demand for consumer electronics such as cellphones for a longer battery life. This paper presents the simulation of half adder, half subtractor, full adder, and the full subtractor. The presented circuit contains NAND gates combining the NMOS and PMOS. These CMOS circuitries has the advantage of lower voltage, lower power consumption, and higher energy efficiency. The NMOS and PMOS were bridge together to produce the desired output. This design provides the CMOS half adder, half subtractor, full adder, and full subtractor using the Tanner EDA software tool. The complete CMOS circuit schematic are described in this paper. The design methods and principles are described thereafter. Simulations have been done with the use of the Tanner EDA tool in a CMOS technology standard and response output was verified comparing the obtained waveform along with its truth table. In comparison with conventional logic truth table, T-Spice output simulation matches with theoretical expectations.**

***Keywords*—Adders, CMOS, logic gates, NMOS, PMOS, Spice, subtractors, Tanner EDA**

## I. INTRODUCTION

In digital electronics, logic gate is an electronic device that performs Boolean logic, wherein the inputs and outputs are in terms of binary numbers. The adders and subtractors of two or more binary digits can be designed through the combinational Boolean logic circuits. Nowadays, low power consumption is an important consideration in designing a system [1-2]. In the design of very large-scale integration or VLSI, the low power consumption of the system is increasing in demand. VLSI has applied in engineering applications such as microcontrollers, communications, a digital image processing, microprocessors, digital signal processing, among others [3-4]. In case that the system is not power efficient, it may consume more power and the system may suffer from working in a higher temperature, lower economic battery life, and additional operation costs. In effect, it may have an adverse influence in the performance of the system and its economic life.

In recent years, the CMOS or complementary metal oxide semiconductor field effect transistors is steadily gaining more attention from the research community that is associated in the design of the VLSI. It has been extensively used in integrated circuit memories, microcontrollers, microprocessors, etc. [4] as an alternative solution for smaller power consumption of system. It has an advantages of higher noise margin, consumes low power, and ease of design [5]. It uses symmetrical pairs and complementary pairs of n-type and p-type, which are the NMOS and PMOS, respectively for digital electronics such as the Boolean logic functions applications.

Nagresh, *et al.* [6] presented a paper on full adder using a CMOS technology, that is good for low power consumption. Gayathri, *et al.* [7] developed a 1-bit full adder using gate diffusion input for static leakage reduction. Kumar and Goyal [8] presented a study of several full adders with the aid of Tanner EDA software. Sharma and Sharma [9] studied the 1-bit half subtractor using CMOS technology by means of DSCH and Microwind software tools. Monikashri, *et al.* [10], Rajni and Dhimari [11], Kumar, *et al.* [12] have studied the 1-bit full subtractor using the CMOS technology by means of a software tool which is Tanner EDA.

The use of CMOS technology can be further applied to a diversified scientific and engineering problems including the minimization of a PCB area in electronic circuits [13] [14], the power electronics and motor drives [15] [16] [17], chip to chip communication [18], robotic [19] [20] [21], renewable energy [22] [23] [24], electric vehicles [25], wireless communications [26] [27] [28] [29] [30], biomedical field [31], chaos [32], and automations [33] [34] [35] [36].

In this paper, a CMOS 1-bit half adder, half subtractor, full adder, and full subtractor is presented using the Tanner EDA software. An assessment is made to verify the performance of the circuit through different logic function input combination and to check the voltage levels output signals. The adders and subtractors are indispensable in digital electronic circuits and logic gates, and these are incorporated in integrated circuits.

This paper is organized as follows. Section II presents the discussion of this project. Simulation results are presented and discussed under Section III. Finally, the conclusion is given in Section IV.

## II. METHODS

### A. General Flowchart

The block diagram shown in Figure 1 illustrate the design process of the system. The schematic circuit was designed in the Tanner EDA software using PMOS and NMOS available in the library. The circuit design will be validated through a T-Spice simulation available in the Tanner EDA. If in case the simulation output response is not good or not satisfactory, then

the circuit design will be re-check and troubleshoot. If in case that the response is in good agreement with theoretical expectations, then simulation will be halted, and all data will be gathered and saved. The overall block flowchart during the design process is illustrated in Figure 1 using Tanner EDA.

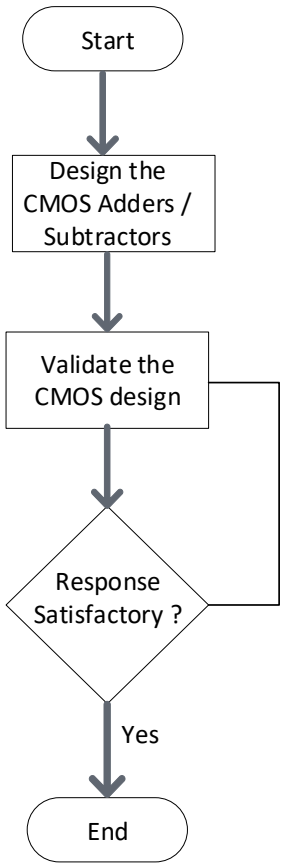


Fig. 1. General design flowchart with Tanner EDA.

### B. *Circuit Schematics*

Figure 2 presents a simple circuitry NAND gate using the cascaded PMOS and NMOS, this serves as the building block in constructing the adders and subtractors in this paper.

Figure 3 shows the half adder circuit using NAND gates. The circuit was composed of twenty transistors to complete the half adder circuit. It shows the connection of the PMOS and NMOS that was bridged together to produce the half adder circuit while Figure 4 shows the schematic diagram of half subtractor using NAND gates. Buffer was incorporated at the output to produce a more stable output response.

The circuits uses PMOS and NMOS to design half adder and half subtractor and full subtractor. The circuit designed used NAND gates to produce the desired outputs, and with the help of the buffer, the output waveforms have been achieved which is more stable than without using a buffer in the design.

Figure 5 illustrates the schematic diagram of the full adder using NAND gates. The PMOS and NMOS are the transistors that were used to create a full adder circuit using CMOS and with the help of truth table, the researchers have verified the results are correct.

Lastly, Figure 6 presents the circuit diagram of a CMOS full subtractor using NAND gates. Just like with the first three diagrams, it also uses PMOS and NMOS to create the NAND gate. Buffers were used to obtain a stable output response as compared to without using a buffer in designed circuit.

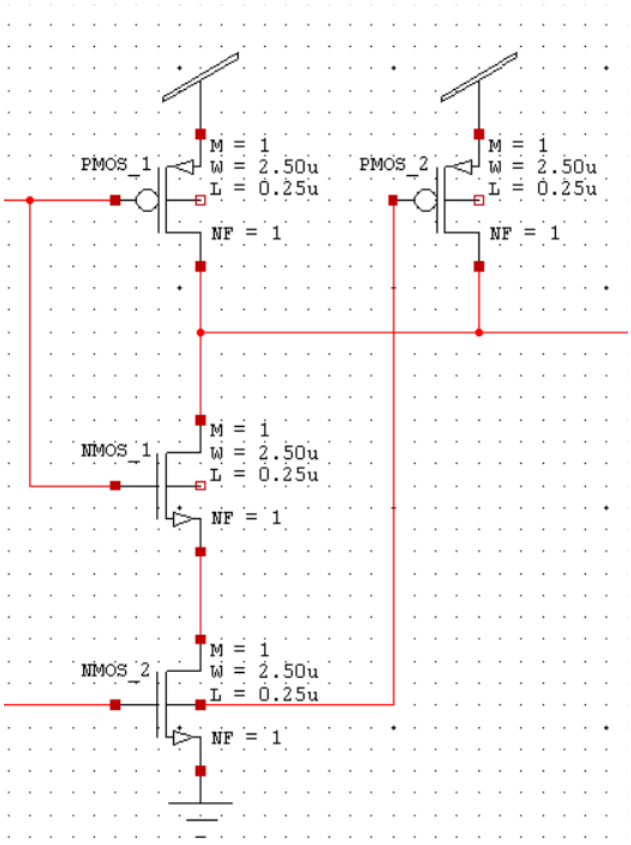


Fig. 2. NAND gate using a bridged PMOS and NMOS.

## III. Simulation Results

The figure below first and second graph in Figure 7 shows the general result of half adder in accordance with a two logic inputs (*i.e.*, 0011 and 0101). The third and fourth graph shows the carry and sum of the half adder system.

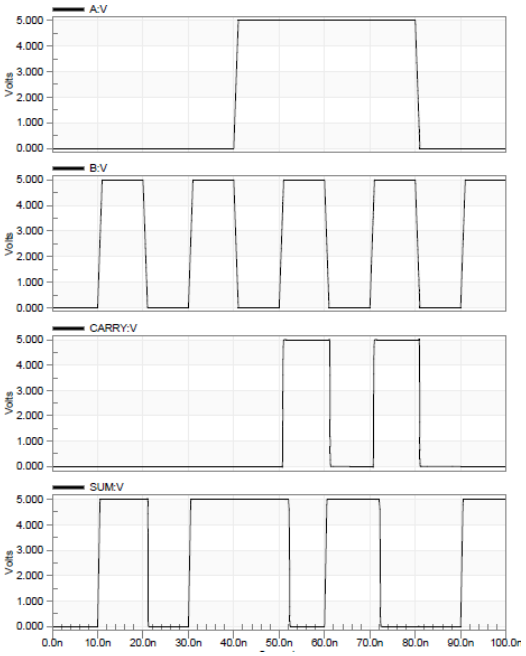


Fig. 7. Half adder response with T-Spice Tanner EDA.

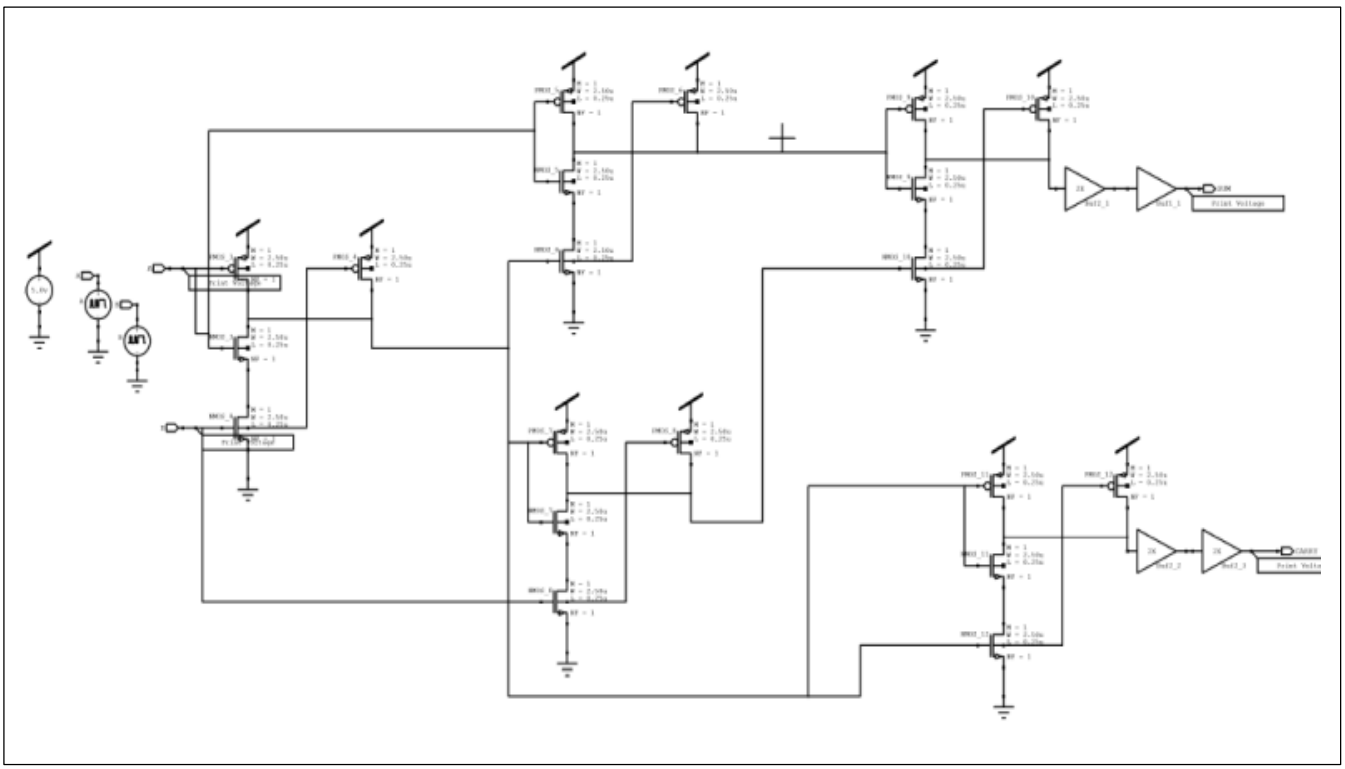

Fig. 3. NAND gates-based half adder CMOS design using Tanner EDA.

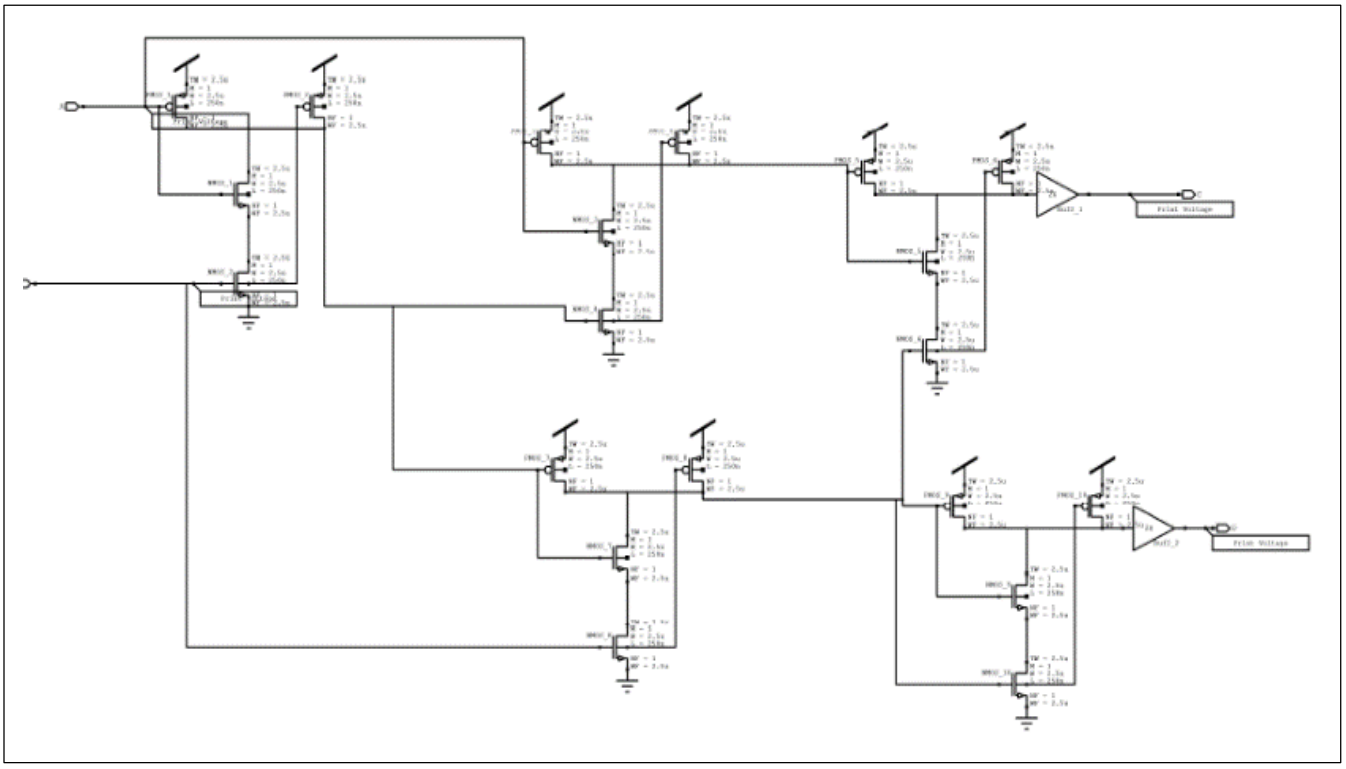

Fig. 4. NAND gates-based half subtractor CMOS design using Tanner EDA.

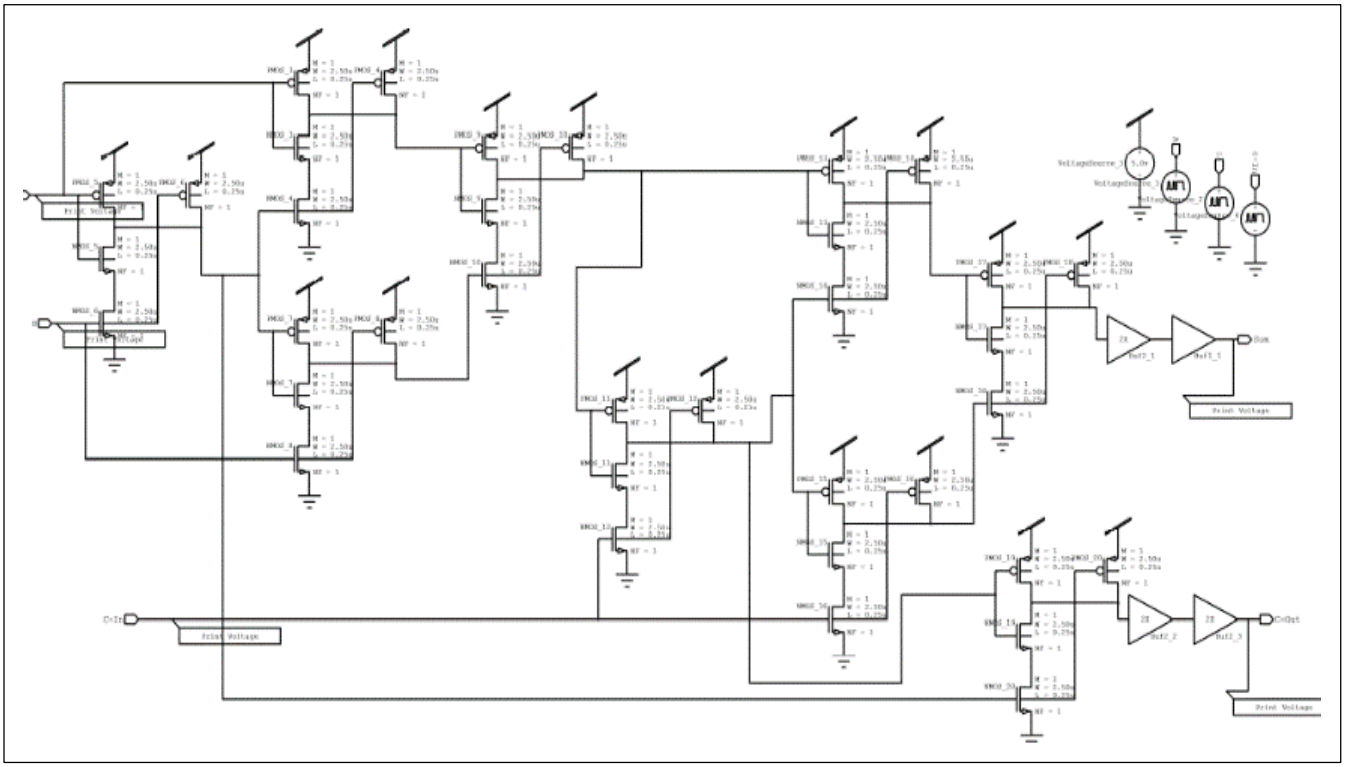

Fig. 5. NAND gates-based full adder CMOS design using Tanner EDA.

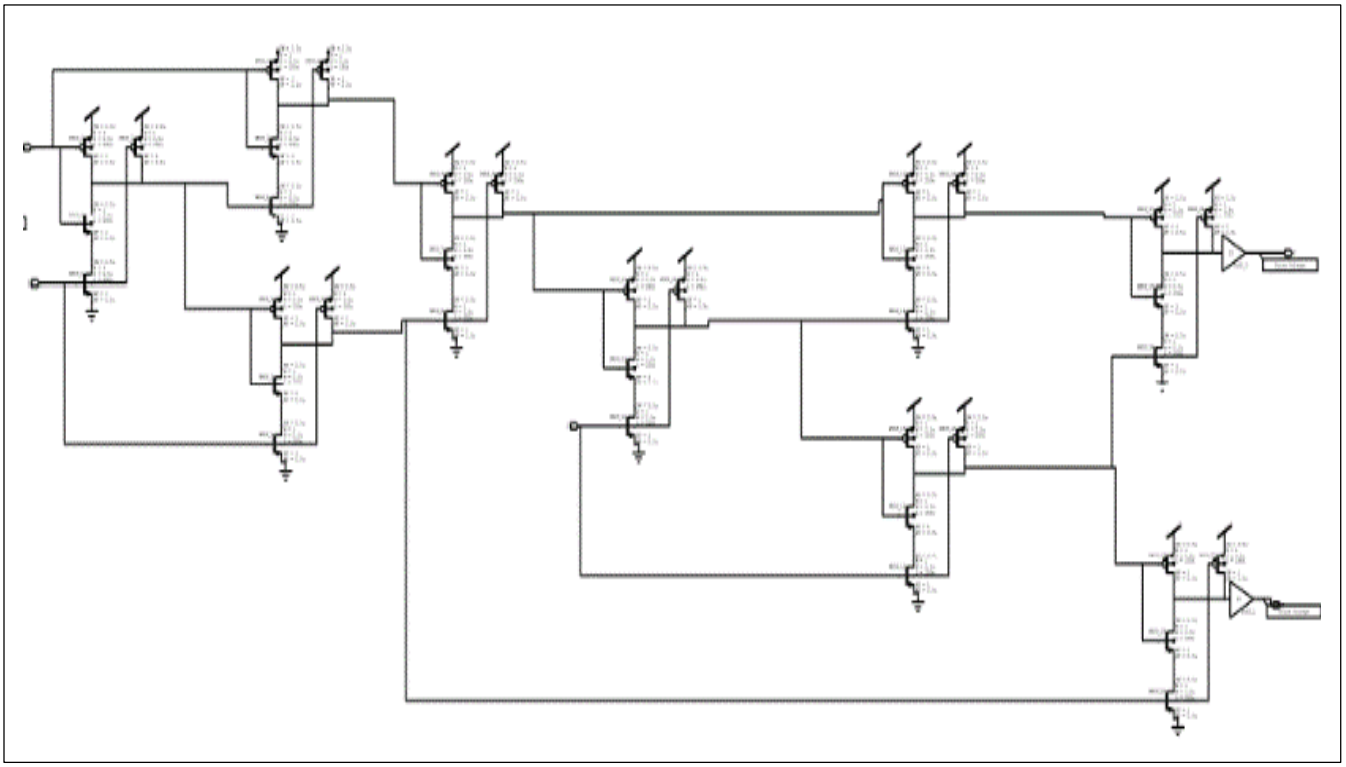

Fig. 6. NAND gates-based full subtractor CMOS design using Tanner EDA.

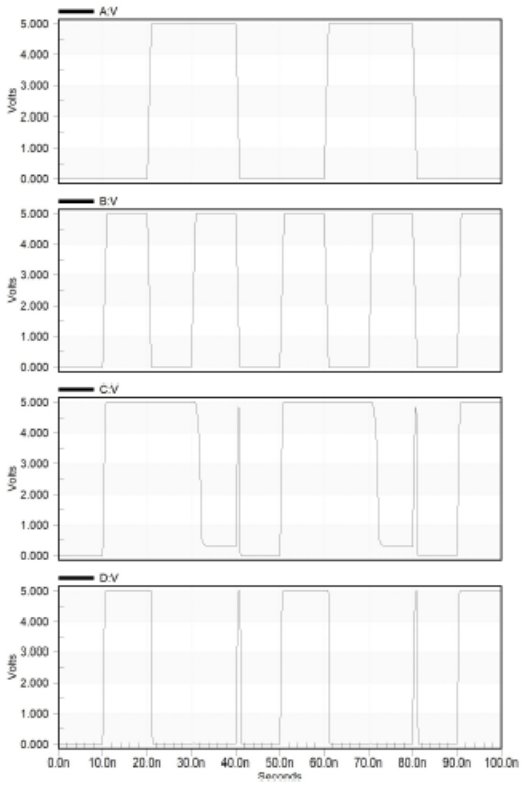


Fig. 8. Half subtractor response with T-Spice Tanner EDA.

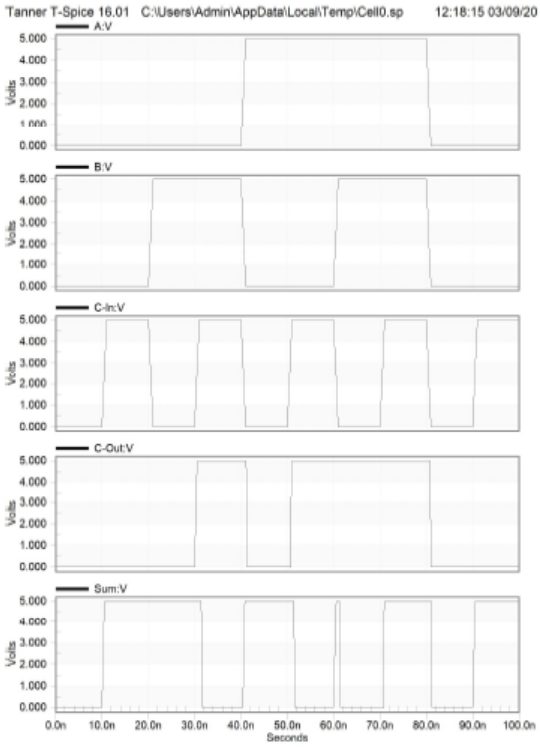


Fig. 9. Full adder response with T-Spice Tanner EDA.

Figure 8 depicts the input and the output results of the half subtractor. The first and second graphs are the inputs while the third and fourth graphs are the borrow and the difference respectively.

While Figure 9 depicts the simulation results of the full adder according with the inputs of 00001111, 00110011 and 01010101. The fourth and fifth graph are the carry and sum.

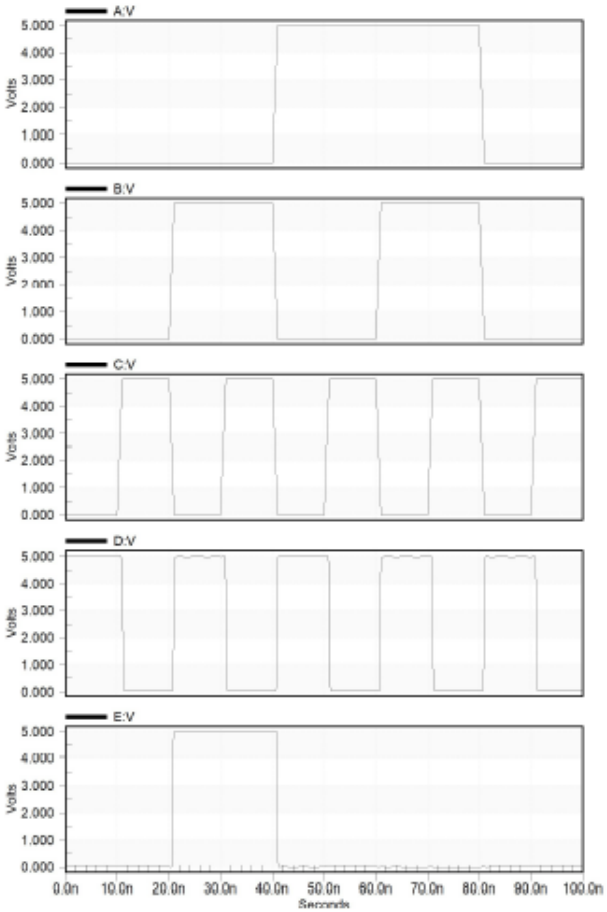


Fig. 10. Full subtractor response with T-Spice Tanner EDA.

Figure 10 presents the result of a full subtractor that was implemented in the Tanner EDA software tool. The first three graphs show the inputs 00001111, 00110011 and 01010101, while the fourth and fifth graphs below on it, are the results.

## IV. CONCLUSION

In this paper, the researchers have designed and tested the functionalities of the half adder, the half subtractor, the full adder, and the full subtractor using the Tanner EDA software tool. The design principles of logic circuits using NAND Gates had been applied to create a CMOS half and full adders also with half and full subtractors circuit through PMOS and NMOS. Simulation studies have been carried out to verify the effectiveness of the proposed scheme. Results reveal that the CMOS circuit design enables the logic function of half adder, half subtractor, the full adder, and full subtractor effectively.

The circuit design is universal and may readily applied to real world engineering applications. Future work will focus on prototype development and applications of the present work.

## REFERENCES

[1] M. Alioto, G. Palumbo, and M. Poli, "Energy consumption in RC tree circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 5, pp. 452–461. July 2006.

[2] A. Wiltgen, K. A. Escobar, A. I. Reis, and R. P. Ribas, "Power consumption analysis in static CMOS gates," in *26TH Symposium on Integrated Circuits and Systems Design (SBCCI)*, pp. 1–6, Curitiba, Brazil, September 2013.

[3] T. Wilmshurst, *Designing Embedded Systems with PIC Microcontrollers 2ed*, 584 pages, Newnes, USA, November 2006. ISBN -13: 978-0750667555

[4] A. A. Beltran Jr., Z. Lontoc, B. Conde, R. Serfa Juan, and J. R. Dizon,

[5] World Congress on Engineering and Technology; Innovation and Its

[6] Sustainability 2018, Springer, Switzerland, September 2019. ISBN

[7] 978-3-030-20903-2

[8] M. H. Rashid, *Microelectronic Circuits: Analysis and Design 3ed*, 1360 pages, Cengage Learning, USA, January 2016. ISBN -13: 978-1305635166

[9] B. B. Rajesh, S. Nagraj, and M. K. Chaitanya, "Full adder using CMOS technology," International Journal of Advanced Trends in Engineering, Science and Technology, vol. 4, special issue no. 1, pp. 208–211. December 2016.

[10] P. K. D. Gayathri, P. Harini, and P. T. Rani, "Design of low power 1-bit full adder using variable sub-threshold voltage at 45nm technology," International Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering, vol. 6, no. 3, pp. 2042–2052. March 2017.

[11] A. Kumar and A. K. Goyal, "Study of various full adders using Tanner EDA tool," International Journal of Computer Science and Technology, vol. 3, no. 1, pp. 581–585. March 2017.

[12] P. Sharma and A. Sharma, "Design and analysis of power efficient PTL half subtractor using 120nm technology," International Journal of Computer Trends and Technology, vol. 7, no. 4, pp. 207–213. January 2014.

[13] T. S. Monikashree, S. Usharani, and J. S. Baligar, "Design and implementation of full subtractor using CMOS 180nm technology," International Journal of Science, Engineering and Technology Research, vol. 3, no. 5, pp. 1421–1426. May 2014.

[14] R. Bukkal and P. Dimri, "1-bit full subtractor using CMOS technique and GDI technique using Tanner EDA tool," International Journal for Scientific Research and Development, vol. 3, no. 4, pp. 1508–1510. July 2015.

[15] G. H. Kumar, K. Gopi, P. Gowtham, and G. N. Balaji, "Area efficient full subtractor based on static 125nm CMOS technology," International Journal of Trend in Scientific Research and Development, vol. 2, no. 6, pp. 1371508–1510. July 2015.

[16] A. A. Beltran Jr., C. D. Hiwatig, N. J. R. Laguna–Agustin, and M. B. Villanueva, "Teaching electronic circuits using altium designer," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 10, pp. 1239–1243, October 2014.

[17] A. A. Beltran Jr., "Design of a linear integrated op amp circuit: an alternative solution to differential equation model of RLC circuit," *Lyceum of the Philippines University Research Journal*, vol. 2, no. 1, pp. 49–65, June 2007.

[18] A. A. Beltran Jr., "Speed control of a three-phase alternating current induction motor using space vector pulse width modulation," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 4, pp. 380–384, April 2014.

[19] A. A. Beltran Jr., "Direct torque control based space vector pulse width modulation of a two level inverter fed three phase alternating current induction motor using Matlab/Simulink," *Institute of Electronics Engineers of the Philippines (IECEP) Journal*, vol. 1, no. 1, pp. 27–36, July 2012.

[20] M. J. P. Diaz, C. E. A. Mariano, and A. A. Beltran Jr., "Accelerometer-based Wave Motion Compensation on Ship Mounted Weaponry," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 5, pp. 588–591, May 2014.

[21] A. A. Beltran Jr. and M. R. Bernardo, "Design and implementation of low power half duplex embedded chip to chip communication via microwire bus interface," *Institute of Electronics Engineers of the Philippines (IECEP) Journal*, vol. 1, no. 1, pp. 19–26, July 2012.

[22] R. E. Tolentino, R. I. A. Casil, B. G. Nia, and A. A. Beltran Jr., "Robotic elbow movement angular position improvement using kalman filter," *Institute of Electronics Engineers of the Philippines (IECEP) Journal*, vol. 3, no. 1, pp. 68–73, May 2014.

[23] A. A. Beltran Jr., R. E. Tolentino, N. C. Javier, and H. Zhang, "MCU-based robotic elbow movement control," *International Journal of Scientific Engineering and Technology*, vol. 4, no. 8, pp. 438–442, August 2015.

[24] A. A. Beltran Jr., C. D. T. Cayao, J. K. V. Delicana, and B. B. Agraan Jr., "Reduced image noise on shape recognition using singular value decomposition for pick and place robotic system," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 4, pp. 385–389, April 2014.

[25] A. A. Beltran Jr. and F. S. Caluyo, "Design and implementation of fuzzy logic controlled uninterruptible power supply integrating renewable solar energy," *International Journal of Engineering Research*, vol. 3, no. 3, pp. 162–166, March 2014.

[26] A. A. Beltran Jr., "Standalone solar PV maximum power point tracking using interval type 2 fuzzy logic," in *IEEE Eurasia Conference on IoT, Communication and Engineering 2019*, pp. 534–537, Yunlin, Taiwan, October 2019.

[27] Y. Y. Hong, A. A. Beltran Jr., and A. C. Paglinawan, "Real-time simulation of maximum power point tracking control using fuzzy logic for standalone PV system," in *IEEE 3RD International Future Energy Conference and ECCE Asia 2017*, pp. 710–715, Kaohsiung, Taiwan, June 2017.

[28] M. A. Z. Amador, M. A. C. Lina, A. G. Aquino, F. A. Gutteres, A. U. Ganggangan, and A. A. Beltran Jr., "Design and implementation of power management system utilizing supercapacitors for hybrid vehicles," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 8, pp. 1074–1077, August 2014.

[29] G. Mappatao, I. M. Z. Bautista, M. K. Orsos, M. A. Ribo, and J. Castillo, "Development of a remote tending system for analog broadcast transmitters," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 15, no. 3, pp. 1474–1484, September 2019.

[30] G. Mappatao, I. M. Z. Bautista, M. K. Orsos, M. A. Ribo, and J. Castillo, "Remote tending of modern broadcast transmitters," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 15, no. 3, pp. 1491–1500, September 2019.

[31] A. C. Paglinawan, L. C. Valiente, A. A. Beltran Jr., A. V. Mabalot, J. A. Verdida, and C. L. D. Marte, "Wireless power transfer using near field communication for mobile devices," in *IEEE 3rd International Future Energy Electronics Conference and ECCE Asia 2017*, pp. 1747 – 1752, Kaohsiung, Taiwan, June 2017.

[32] A. A. Beltran Jr., F. I. Alano, V. B. Alvarez, R. J. D. Habab, and P. M. P. Buay, "A simulation research in linear beam forming transmission," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 12, pp. 1431 – 1435, December 2014.

[33] A. A. Beltran Jr., G. Tan, S. Y. Castriciones, K. Cuerdo, A. Valdez, and J. J. Vega, "Design and implementation of an emergency datacasting system using 2-meter amateur radio band," in *IEEE International Conference on Smart Technology and Applications 2020*, pp. 1–5, Surabaya, Indonesia, February 2020.

[34] A. U. Ganggangan, A. A. Beltran Jr., E. C. Barreto, P. F. Hernandez, P. E. P. De Villa, and M. T. A. M. Cabatac, "Chest worn pulse oximeter integrating NI USRP with GPS disciplined clock transmitter," *International Journal of Scientific Engineering and Technology*, vol. 4, no. 1, pp. 10 – 14, January 2015.

[35] A. A. Beltran Jr., "A new lorenz unlike chaotic attractor," in *2ND International E-Conference on Emerging Trends in Technology 2014*, pp. 16–23, Bhopal, India, February 2014.

[36] A. A. Beltran Jr., A. C. Clavero, J. M. B. De Vera, P. A. P. Lopez, C. A. Mueca, N. A. Pempena IX, and A. Z. D. Roxas, "Arduino based food and water dispenser for pets with GSM technology control," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 4, pp. 231 – 234, April 2014.

[37] J. M. M. Baroro, M. I. Alipio, M. L. T. Huang, T. M. Ricamara, and A. A. Beltran Jr., "Automation of packaging and material handling using programmable logic controller," *International Journal of Scientific Engineering and Technology*, vol. 3, no. 6, pp. 767–770, June 2014.

[38] J. L. G. Medialdea, M. E. C. Manamparan, M. G. M. Sorita, E. L. Ponce, and A. A. Beltran Jr., "A novel thermal gas analyzer using adaptive neuro-fuzzy inference system (ANFIS)," *Institute of Electronics Engineers of the Philippines (IECEP) Journal*, vol. 2, no. 1, pp. 27–31, June 2013.

[39] R. I. A. Casil, E. D. Dimaunahan, M. E. C. Manamparan, B. G. Nia, and A. A. Beltran Jr., "A DSP based vector quantized mel frequency cepstrum coefficients for speech recognition," *Institute of Electronics Engineers of the Philippines (IECEP) Journal*, vol. 3, no. 1, pp. 1–5, May 2014.